IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for managing dataflow through a processing system, comprising:

gathering writes in a buffer before transmitting a burst of writes over an external bus;

monitoring the buffer to determine a number of writes in the buffer and whether the number of writes in the buffer exceed a predetermined threshold;

identifying an error condition when the number of writes in the buffer exceed the predetermined threshold; and

providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold;

wherein the providing control over a rate of a number of writes provided to the buffer further comprises providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto.

2. (Original) The method of claim 1, wherein the providing control further comprises slowing writes to the buffer when the writes in the buffer exceed the predetermined threshold.

3. (Original) The method of claim 1, wherein the gathering writes in a buffer before transmitting a burst of writes over an external bus further comprises transmitting a burst of writes over a bus.

4. (Original) The method of claim 1 further comprising initiating error recovery in response to the writes in the buffer exceeding the predetermined threshold.

5. (Original) The method of claim 1 further comprising providing an arbitration signal for controlling access to the external bus in response to the comparison of the writes in the buffer to the predetermined threshold.

6. (Canceled)

7. (Currently Amended) The method of claim [[6]] 1, wherein the providing a vector to a register further comprises asserting an interrupt line to the register to provide an indication of an almost full state for the buffer in response to the vector.

8. (Original) The method of claim 1 further comprising clearing the buffer when the writes in the buffer exceed the predetermined threshold.

9. (Original) The method of claim 1 further comprising providing a timeout signal for indicating when a transaction is not cleared from the buffer within a predetermined amount of time and clearing the buffer and external bus transactions in response thereto.

10. (Currently Amended) The method of claim 1 further comprising determining whether an external interface is hung based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer and clearing the buffer and external bus transactions when ~~an~~ the external interface is hung.

11. (Currently Amended) A processing system, comprising:

a processor for generating writes over a processor bus;

a buffer, coupled to the processor bus, for gathering the writes before transmitting a burst of writes over an external bus; ~~and~~

a bus monitor, coupled to the write buffer, for determining a number of writes in the buffer, identifying an error condition when the number of writes in the buffer exceed the predetermined threshold, and providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold; and

a register, the buffer monitor providing a vector to the register, the processor scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto.

12. (Original) The processing system of claim 11 further comprising an external interface coupled to the buffer, the external interface linking the buffer to the external bus.

13. (Original) The processing system of claim 11, wherein the external bus comprises a PCI-X bus.

14. (Original) The processing system of claim 11 further comprising a processor interface coupled to the buffer, the processor interface linking the buffer to a processor bus.

15. (Original) The processing system of claim 11, wherein the processor initiates error recovery in response to the writes in the buffer exceeding the predetermined threshold.

16. (Original) The processing system of claim 11, wherein the buffer monitor provides an arbitration signal for controlling access to an external bus in response to the comparison of the writes in the buffer to the predetermined threshold.

17. (Original) The processing system of claim 11, wherein the buffer monitor comprises bus arbitration and control logic for controlling the movement of data onto the external bus.

18. (Original) The processing system of claim 17, wherein the buffer bursts the writes onto the external bus.

19. (Canceled)

20. (Currently Amended) The processing system of claim [[19]] 11, wherein the buffer monitor provides the vector by asserting an interrupt line to the register to provide an indication of an almost full state for the buffer.

21. (Currently Amended) The processing system of claim [[19]] 11, wherein the vector represents an almost full state for the buffer.

22. (Original) The processing system of claim 11, wherein the buffer monitor monitors the buffer, the external bus, and the processor bus for error conditions.

23. (Previously Presented) The processing system of claim 22, wherein the error conditions comprise anticipated error conditions based upon detecting a static buffer pointer representing a lack of movement of writes in the buffer.

24. (Original) The processing system of claim 11, wherein the buffer monitor provides a buffer pointer to the processor to control the movement of writes from the processor to the buffer.

25. (Original) The processing system of claim 11, wherein the processor clears the buffer when the writes in the buffer exceed the predetermined threshold.

26. (Original) The processing system of claim 11, wherein the buffer monitor comprises a timer for providing a timeout signal to the processor when a transaction on the processor bus is not cleared within a predetermined amount of time.

27. (Currently Amended) A processing system, comprising:

a memory for gathering writes for burst transmission over an external bus; ~~and~~

a processor, coupled to the memory, the processor being configured for monitoring the memory to determine a number of writes in the buffer and whether the number of writes in the memory exceed a predetermined threshold, identifying an error condition when the number of writes in the buffer exceed the predetermined threshold, and providing control over a rate of a number of writes provided to the memory in response to the monitored number of writes in the memory and the predetermined threshold; and

a register, wherein a vector is provided to the register, the processor scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto..

28. (Currently Amended) A program storage device readable by a computer, the program storage device tangibly embodying one or more programs of instructions executable by the computer to perform a method for managing dataflow through a processing system, the method comprising:

gathering writes in a buffer before transmitting a burst of writes over an external bus;

monitoring the buffer to determine a number of writes in the buffer and whether the number of writes in the buffer exceed a predetermined threshold;

identifying an error condition when the number of writes in the buffer exceed the predetermined threshold; and

providing control over a rate of a number of writes provided to the buffer in response to the monitored number of writes in the buffer and the predetermined threshold;

wherein the providing control over a rate of a number of writes provided to the buffer further comprises providing a vector to a register and scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto.

29. (Currently Amended) A processing system, comprising:

means for gathering writes for burst transmission over an external bus; and

means, coupled to the means for gathering, for monitoring the means for gather to determine a number of writes in the buffer and whether the number of writes in the means for gathering exceed a predetermined threshold, for identifying an error condition when the number of writes in the buffer exceed the predetermined threshold, and for providing control over a rate of a number of writes provided to the means for gathering in response to the monitored number of writes in the buffer and the predetermined threshold; and

a register, wherein a vector is provided to the register, the processor scanning the register for the vector to determine when a number of writes in the buffer is static and to slow writes to the buffer in response thereto..